In the Claims:

1-24. (canceled)

25. (previously added)An integrated circuit comprising:

A. functional circuits;

B. a serial data input lead and a serial data output lead;

C. at least one serial scan path of scan registers, the scan registers of the serial scan path being coupled between the serial data input lead and the serial data output lead and the serial scan path being coupled to the functional circuits;

D. a protocol selection memory coupled to the serial scan path, the protocol selection memory having at least one storage location to store a protocol selection signal; and

E. an event control circuit coupled to the serial scan path, the event control circuit including a protocol input connected to the protocol selection memory, an event input lead and an event output lead.

26. (previously added)The integrated circuit of claim 25 in which the protocol selection memory receives the protocol selection signal from the at least one serial scan path.

27. (previously added)The integrated circuit of claim 26 in which the event input lead receives an event signal, the event signal having either an active state or an inactive state, the event control circuit initiating a protocol on the functional circuitry when the event input lead receives the active event signal, the protocol being defined by the protocol selection signal.

28. (previously added)The integrated circuit of 27 including a comparator on the integrated circuit, the comparator having plural functional input leads coupled to

the functional circuit, plural expected data input leads coupled to an expected data memory, and an output coupled to the event input lead, so that when at least some of the signals on the functional input leads match corresponding signals on the expected data input leads, the comparator produces the active event signal on the event input lead.

29. (previously added) The integrated circuit of claim 28 in which the event input lead receives the event signal from external of the integrated circuit.

30. (previously added) The integrated circuit of claim 25 in which the event input lead receives an event signal, the event signal having either an active state or an inactive state, the event control circuit initiating a protocol on the functional circuitry when the event input lead receives the active event signal, the protocol being defined by the protocol selection signal.

31. (previously added) The integrated circuit of claim 27 including a comparator on the integrated circuit and in which the event input lead receives the event signal from the comparator.

32. (previously added) The integrated circuit of claim 25 in which the event input lead receives an event signal from external of the integrated circuit.

33. (previously added) The integrated circuit of claim 25 including circuitry for performing plural protocols, and the protocol being selected by the protocol selection signal.

34. (previously added) The integrated circuit of claim 33 including a data register coupled to the functional circuits for storing data from the functional circuits during the selected protocol.

35. (previously added)The integrated circuit of claim 34 in which the data register is coupled to the serial data output lead to shift the data stored in the data register out of the serial data output lead during the protocol.

36. (previously added)The integrated circuit of claim 25 in which the event control circuit includes combinational logic circuitry coupled to the protocol selection memory and the event input lead.

37. (previously added)The integrated circuit of claim 25 including an enable signal register coupled to the at least one serial scan path, and the event control circuit including combinational logic circuits coupled to the protocol selection memory, the event input lead, and the enable signal register.

38. (previously added)The integrated circuit of claim 25 in which the event control circuit further includes a second event input lead, the second event input lead coupled to receive a second event signal from external of the integrated circuit, the event input lead being coupled to receive an event signal from internal the integrated circuit, the event signal and the second event signal each having either an active state or an inactive state, and the integrated circuit further including a comparator on the integrated circuit having plural first input leads coupled to receive signals from the functional circuits, plural second input leads coupled to receive expected data signals from an expected data memory, and an output coupled to the event input lead, so that when at least some of the signals on the first inputs match corresponding signals on the second input leads the comparator produces an active state event signal on the event input lead, and where the event control circuit initiates a protocol on the functional

circuitry when at least one of the event input lead and the second event input lead receive an active state event signal, the protocol being defined by the protocol selection signal.

39. (previously added) Observation circuits comprising:

A. a serial scan signal input lead;

B. a serial scan signal output lead;

C. a serial clock signal input lead;

D. a mode select signal input lead;

E. a serial scan path coupled between the serial scan signal input lead and the serial scan signal output lead;

F. an access port circuit coupled to the serial scan path, to the mode select signal input lead, and to the serial clock signal input lead;

G. a protocol selection memory coupled to the serial scan path and including at least one storage location to store a protocol selection signal; and

H. an event control circuit having a protocol input coupled to the protocol selection memory, an event input lead, and an event output lead.

40. (previously added) The observation circuits of claim 39 in which the protocol selection memory receives the protocol selection signal from the serial scan path.

41. (previously added) The observation circuits of claim 40 in which the event input lead receives an event signal, the event signal having either an active state or an inactive state, the event control circuit initiating a protocol when the event input lead receives the active event signal, the protocol defined by the protocol selection signal.

42. (previously added) The observation circuits of claim 41 including a comparator, the comparator having plural data input leads coupled to a circuit being observed, plural expected data input leads coupled to an expected data memory, and an output coupled to the event input lead, so that when at least some of the signals on the data input leads match corresponding signals on the expected data input

leads, the comparator produces the active event signal on the event input lead.

43. (previously added)The observation circuits of claim 41 in which the event input lead receives the event signal from external of the observation circuits.

44. (previously added)The observation circuits of claim 39 in which the event input lead receives an event signal, the event signal having either an active state or an inactive state, the event control circuit initiating a protocol when the event input lead receives the active event signal, the protocol defined by the protocol selection signal.

45. (previously added)The observation circuits of claim 44 including a comparator and in which the event input lead receives the event signal from the comparator.

46. (previously added)The observation circuits of claim 39 in which the event input lead receives an event signal from external of the observation circuits.

47. (previously added)The observation circuits of claim 39 including circuitry for performing plural protocols, and the protocol being selected by the protocol selection signal.

48. (previously added)The observation circuits of claim 47 including a data register coupled to a circuit being observed for storing data from the circuit being observed during the selected protocol.

49. (previously added)The observation circuits of claim 48 in which the data register is coupled to the serial data output lead to shift the data stored in the data register out of the serial data output lead during the protocol, and in which the access port includes control outputs responsive

to the serial clock signal and the mode select signal and coupled to the data register to control the shifting of data out of the data register and to serial data output lead.

50. (previously added)The observation circuits of claim 39 in which the event control circuit includes combinational logic circuitry coupled to the protocol selection memory and the event input lead.

51. (previously added)The observation circuits of claim 39 including an enable signal register coupled to the serial scan path, and the event control circuit including combinational logic circuits coupled to the protocol selection memory, the event input lead, and the enable signal register.

52. (previously added)The observation circuits of claim 39 in which the event control circuit further includes a second event input lead, the second event input lead coupled to receive a second event signal from external of the observation circuits, the event input lead being coupled to receive an event signal from internal the observation circuits, the event signal and the second event signal each having either an active state or an inactive state, and the observation circuits further including a comparator having plural first input leads coupled to receive signals from a circuit being observed, plural second input leads coupled to receive expected data signals from an expected data memory, and an output coupled to the event input lead, so that when at least some of the signals on the first inputs match corresponding signals on the second input leads, the comparator produces an active state event signal on the event input lead, and where the event control circuit initiates a protocol when at least one of the event input lead and the second event input lead receive an active state

event signal, the protocol being defined by the protocol selection signal.

53. (previously added) An integrated circuit comprising:

A. a functional circuit;

B. a serial data input lead and a serial data output lead;

C. a serial scan path of scan registers coupled between the serial data input lead and the serial data output lead;

D. a scan clock signal lead and a scan mode signal lead;

E. an access port having a first input coupled to the scan clock signal lead, a second input coupled to the scan mode signal lead, and at least one control output coupled to the serial scan path;

F. a protocol selection memory coupled to the serial scan path and having at least one storage location;

G. an event input lead; and

H. event control circuitry having an input coupled to the event input lead, an input coupled to the protocol selection memory, and an output coupled to the functional circuit.

54. (previously added) The integrated circuit of claim 53 in which the protocol selection memory receives the protocol selection signal from the serial path of scan registers.

55. (previously added) The integrated circuit of claim 54 in which the event input lead receives an event signal, the event signal having either an active state or an inactive state, the protocol circuitry initiating a protocol on the functional circuitry when the event input lead receives the active event signal, the protocol defined by the protocol selection signal.

56. (previously added) The integrated circuit of 55 including a comparator on the integrated circuit, the comparator having plural functional input leads coupled to

the functional circuit, plural expected data input leads coupled to an expected data memory, and an output coupled to the event input lead, so that when at least some of the signals on the functional input leads match corresponding signals on the expected data input leads, the comparator produces the active event signal on the event input lead.

57. (amended) The integrated circuit of claim ~~57~~ 53 in which the event input lead receives the event signal from external of the integrated circuit.

58. (previously added) The integrated circuit of claim 53 in which the event input lead receives an event signal, the event input signal having either an active state or an inactive state, the protocol circuitry initiating a protocol on the functional circuitry when the event input lead receives the active event signal, the protocol defined by the protocol selection signal.

59. (previously added) The integrated circuit of claim 58 including a data register coupled to the functional circuits for storing data from the functional circuits during the selected protocol.

60. (previously added) The integrated circuit of claim 59 in which the data register includes a serial input coupled to the serial data input lead, a serial output coupled to the serial data output and a control input coupled to the control output of the access port, the data register operable to shift the data stored in the data register out of the serial data output lead during the protocol in response to signals received on the control input.

61. (previously added) The integrated circuit of claim 60 in which the data register is also operable to shift data into the data register from the serial data input lead during the

protocol in response to signals received on the control input.

62. (previously added) The integrated circuit of claim 53 in which the event control circuit includes combinational logic circuitry coupled to the protocol selection memory and the event input lead.

63. (previously added) The integrated circuit of claim 53 including an enable signal register coupled to the serial scan path, and the event control circuit including combinational logic circuits coupled to the protocol selection memory, the event input lead, and the enable signal register.